Integrated Memristor Control and Crossbar Array Design using TSMC 28 nm Technology

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The crossbar array architecture with memristors is used for vector matrix multiplication (VMM) and acts as kernels in neuromorphic computing [1]. A conductance control scheme with a regulated voltage source will improve the architecture and reduce the possible potential divider effects due to line resistances [2]. A change in conductance is also possible with the provision of a regulated current source and measuring the voltage across the memristor. A regulated 2T1R memristor conductance control architecture is proposed in this work, which avoids the potential divider effect and virtual ground scenario in a regular crossbar scheme, as well as conductance control by passing a regulated current through memristors as shown in Fig. 1. The sneak path current is not allowed to enter by providing the ground potential to both terminals of memristors. The control architecture with a 2×2 array size is successfully taped out in a 28 nm CMOS technology. The MEMCTRL block includes a core corresponding to the intended conductance control architecture, incorporating voltage mode control and current mode control in two rows, core biasing circuits, resistive DAC, and a digital control block for the pulse width generator with chip layout shown in Fig. 2. The pulse width control and digital configurations for selecting rows and columns are done with an integrated RISC-V processor, running with a clock frequency of up to 100 MHz. Alternatively, direct access is enabled through a JTAG programming interface. The readout circuit is implemented with a current source SAR ADC. The overall size of the chip is 1.4 mm by 1.0 mm, of which the memristor control circuit incorporates an area of 0.4 mm by 0.5 mm. The memristors are not co-integrated in this architecture, however, pins are provided for accessing external memristors. The chip is expected to be delivered in summer 2024 and a first insight into the measurements will be provided.

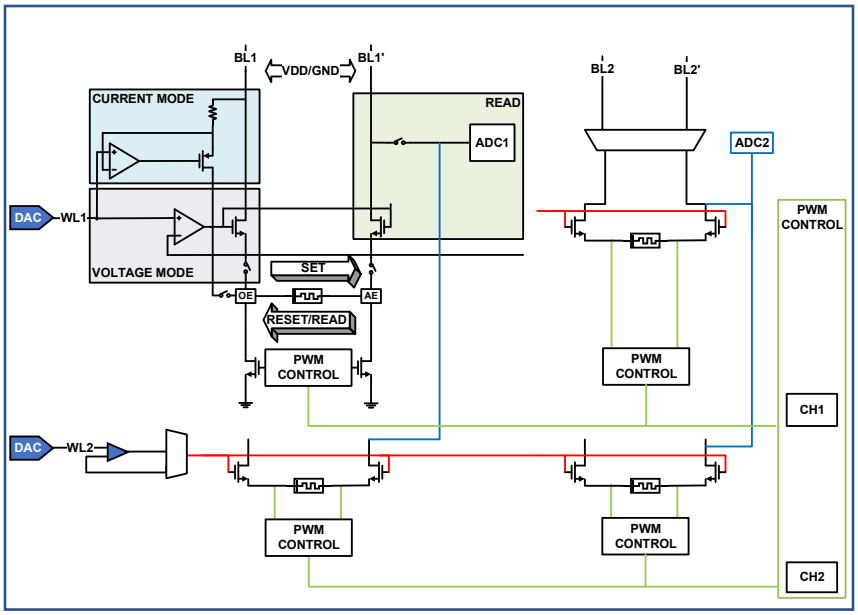

Figure 1. 2T1R memristor conductance control architecture for array size of 2×2

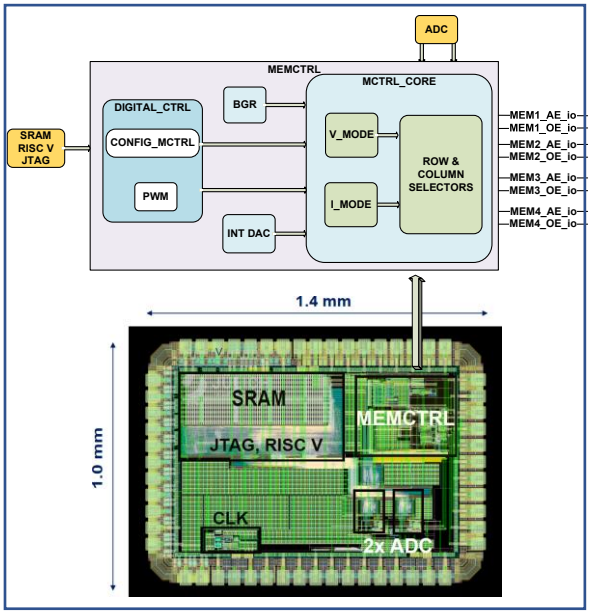

Figure 2. Chip layout of the manufactured memristor control demonstrator with annotated blocks

References

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